# CLAIMS

What is claimed is:

1. A data detection circuit, comprising:

a transient detector that senses transient events in data;

a first data detector path that applies a first equalization target to generate a first bit stream from said data;

a second data detector path that applies a second equalization target to generate a second bit stream from said data; and

a baseline correction circuit that generates a baseline correction signal using said first bit stream when said transient detector does not sense said transient events and said second bit stream when said transient detector senses said transient events.

2. The data detection circuit of Claim 1 wherein said transient events are thermal asperity events.

3. The data detection circuit of Claim 1 wherein said first equalization target is a non-DC free equalization target and said second equalization target is a DC-free equalization target.

4. The data detection circuit of Claim 1 wherein said first data detector path includes:

a first finite impulse response (FIR) equalizer that receives said data; and

a first data detector that receives an output of said first FIR equalizer.

5. The detection circuit of Claim 4 wherein said first data detector includes at least one of a Viterbi detector, a decision feedback equalizer, a peak detector, a threshold detector, and a maximum aposteriori detector.

6. The data detection circuit of Claim 1 wherein said second data detector path includes:

a second finite impulse response (FIR) equalizer; and

a second data detector that receives an output of said second FIR equalizer.

7. The detection circuit of Claim 6 wherein said second data detector includes at least one of a Viterbi detector, a decision feedback equalizer (DFE), a peak detector, a threshold detector, a maximum aposteriori probability (MAP) detector, a list decoding detector, and a sequential decoding detector.

8. The data detection circuit of Claim 4 further comprising a summer that has a first input that communicates with an output of said first FIR equalizer, wherein an output of said summer communicates with said first data detector and said baseline correction circuit, and said baseline correction circuit outputs said baseline correction signal to a second input of said summer.

9. The data detection circuit of Claim 4 wherein said second data detector path includes said first finite impulse response (FIR) filter and further comprises:

a second filter that has an equalization target with a (1-D) factor and that communicates with an output of said first FIR filter; and

a second data detector that communicates with an output of said second filter.

10. The data detection circuit of Claim 1 further comprising:

a first finite impulse response (FIR) equalizer;

a second filter that has an equalization target with a (1-D) factor and that communicates with an output of said first FIR equalizer;

a first data detector that selects one of said output of said first FIR equalizer and said output of said second filter; and

wherein said first data detector path includes said first FIR equalizer and said first data detector and wherein said second data detector path includes said first FIR filter, said second filter and said first data detector.

11. The data detection circuit of Claim 10 wherein said first data detector is at least one of a Viterbi detector, a decision feedback equalizer (DFE), a peak detector, a threshold detector, a maximum aposteriori probability (MAP) detector, a list decoding detector, and a sequential decoding detector.

12. A system comprising the data detection circuit of Claim 1 and further comprising:

a perpendicular recording system including a read signal preamplifier;

a front end that receives a read signal from a read signal preamplifier and that communicates with said transient detector; and

a sampler that communicates with said front end.

13. The data detection circuit of Claim 4 wherein said baseline correction circuit includes:

a delay element that selectively receives an output of said first FIR equalizer;

a reconstruction filter that selectively receives one of said first and second bit streams from said first and second data detector paths, respectively;

a summer that has a first input that receives an output of said delay element and a second input that receives an output of said reconstruction filter; and

an accumulator that receives an output of said first summer and that generates said baseline correction signal.

14. A system comprising the data detection circuit of Claim 1 and further comprising:

a magnetic medium having sectors, wherein said baseline correction circuit uses said second bit stream until said sector ends when said transient detector senses said transient events during said sector.

15. A data detection circuit, comprising:

a thermal asperity detector that senses said thermal asperity events;

a data detector that communicates with said thermal asperity detector and that selectively employs a non-DC free equalization target to generate a first bit stream when said thermal asperity events are not sensed and a DC-free equalization target to generate a second bit stream when said thermal asperity events are sensed; and

a baseline correction circuit that generates a baseline correction signal using said first bit stream when said thermal asperity events are not sensed and said second bit stream when said thermal asperity events are sensed.

16. The data detection circuit of Claim 15 wherein said data detector comprises a first data detector path including:

a first finite impulse response (FIR) equalizer that receives said data; and

a first data detector that receives an output of said first FIR equalizer.

17. The data detection circuit of Claim 16 wherein said first data detector includes at least one of a Viterbi detector, a decision feedback equalizer (DFE), a peak detector, a threshold detector, a maximum aposteriori probability (MAP) detector, a list decoding detector, and a sequential decoding detector.

18. The data detection circuit of Claim 15 wherein said data detector comprises a second data detector path including:

a second finite impulse response (FIR) equalizer; and

a second data detector that receives an output of said second FIR equalizer.

19. The data detection circuit of Claim 18 wherein said first data detector includes at least one of a Viterbi detector, a decision feedback equalizer (DFE), a peak detector, a threshold detector, a maximum aposteriori probability (MAP) detector, a list decoding detector, and a sequential decoding detector.

20. The data detection circuit of Claim 16 further comprising a summer that has a first input that communicates with an output of said first FIR equalizer, wherein an output of said summer communicates with said first data detector and said baseline correction circuit, and said baseline correction circuit outputs said baseline correction signal to a second input of said summer.

21. The data detection circuit of Claim 16 wherein said data detector includes a second data detector path including said first finite impulse response (FIR) filter and further comprising:

a second filter that has an equalization target with at least one (1-D) factor and that communicates with an output of said first FIR filter; and

a second data detector that communicates with an output of said second filter.

22. The data detection circuit of Claim 21 wherein said second data detector includes at least one of a Viterbi detector, a decision feedback equalizer (DFE), a peak detector, a threshold detector, a maximum aposteriori probability (MAP) detector, a list decoding detector, and a sequential decoding detector.

23. The data detection circuit of Claim 15 wherein said data detector comprises:

a first finite impulse response (FIR) equalizer;

a second filter that has an equalization target with at least one (1-D) factor and that communicates with an output of said first FIR equalizer; and

a first data detector that selectively communicates with said output of said first FIR equalizer and said output of said second filter;

wherein when said thermal asperity is not sensed, said data detector uses a first data detector path that includes said first FIR equalizer and said first data detector and wherein when said thermal asperity is sensed, said data detector uses a second data detector path that includes said first FIR filter, said second filter and said first data detector.

24. The data detection circuit of Claim 23 wherein said first data detector includes at least one of a Viterbi detector, a decision feedback equalizer (DFE), a peak detector, a threshold detector, a maximum aposteriori probability (MAP) detector, a list decoding detector, and a sequential decoding detector.

25. A system comprising the data detection circuit of Claim 15 and further comprising:

a perpendicular recording system with a read signal preamplifier;

a front end that receives a read signal from said read signal preamplifier and that communicates with said thermal asperity detector; and

a sampler that communicates with said front end.

26. The data detection circuit of Claim 16 wherein said baseline correction circuit includes:

a delay element that selectively receives an output of said first FIR equalizer;

a reconstruction filter that selectively receives one of said first and second bit streams from said data detector, respectively;

a summer that has a first input that receives an output of said delay element and a second input that receives an output of said reconstruction filter; and

an accumulator that receives an output of said first summer and that generates said baseline correction signal.

27. A system comprising the data detection circuit of Claim 15 and further comprising:

a magnetic medium having sectors, wherein said baseline correction circuit uses said second bit stream until said sector ends when said transient detector senses said transient events during said sector.

28. A perpendicular recording system, comprising:

a perpendicular recording head that generates a read data signal from sectors of a magnetic medium, wherein said read data signal includes at least one of data and transients;

a transient detector that generates a transient detect signal when said transients are detected in said read data signal; and

a detection circuit that detects data in said read data signal, that generates a first detected data signal when said transient detect signal is not generated, and that filters said read data signal and generates a second detected data signal when said transient detect signal is generated,

wherein when transients are detected during a sector, said detection circuit continues using said second detected data signal until said sector ends.

29. The perpendicular recording system of Claim 28 wherein said detection circuit includes:

a first path with a filter and a first data detector;

a second path with a second data detector; and

a selector that communicates with said transient detector and that switches between said first and second paths based on said transient detect signal.

30. The perpendicular recording system of Claim 28 wherein said detection circuit includes:

a filter having an input and an output;

a selector that communicates with said transient detector and said filter and that bypasses said filter when said transient detect signal is present; and

a first detector that receives one of the read data signal from said switch and a filtered read data signal from said filter.

31. The perpendicular recording system of Claim 29 wherein said first data detector includes at least one of a Viterbi detector, a decision feedback equalizer (DFE), a peak detector, a threshold detector, a maximum aposteriori probability (MAP) detector, a list decoding detector, and a sequential decoding detector.

32. The perpendicular recording system of Claim 29 wherein said second data detector includes at least one of a Viterbi detector, a decision feedback equalizer (DFE), a peak detector, a threshold detector, a maximum aposteriori probability (MAP) detector, a list decoding detector, and a sequential decoding detector.

33. The perpendicular recording system of Claim 29 wherein said filter has a high pass filter characteristic.

34. The perpendicular recording system of Claim 28 further comprising a discrete channel circuit that interfaces with said perpendicular recording head and that amplifies said read data signal.

35. The perpendicular recording system of Claim 34 wherein said discrete channel circuit is an analog circuit that includes an analog preamplifier, a filter that communicates with said analog preamplifier, and a forward equalizer that communicates with said filter.

36. The perpendicular recording system of Claim 34 wherein said discrete channel circuit is a digital circuit that includes:

a sampling circuit that digitizes said read data signal;

a FIR filter that receives said digitized read data signal from said sampling circuit, that attenuates out of band noise and that generates an attenuated read data signal; and

an equalizer that receives said attenuated read data signal and that removes intersymbol interference (ISI) from said attenuated read data signal.

37. A data detection circuit, comprising:

transient detecting means for sensing transient events in data;

first data detecting means for applying a first equalization target to generate a first bit stream from said data;

second data detecting means for applying a second equalization target to generate a second bit stream from said data; and

baseline correction means for generating a baseline correction signal using said first bit stream when said transient detecting means does not sense said transient events and said second bit stream when said transient detecting means senses said transient events.

38. The data detection circuit of Claim 37 when said transient events are thermal asperity events.

39. The data detection circuit of Claim 37 wherein said first equalization target is a non-DC free equalization target and said second equalization target is a DC-free equalization target.

40. The data detection circuit of Claim 37 wherein said first data detecting means includes:

first finite impulse response (FIR) means for equalizing input data; and

first data detecting means for detecting data in an output of said first FIR means.

41. The detection means of Claim 40 wherein said first data detecting means includes at least one of a Viterbi detector, a decision feedback equalizer (DFE), a peak detector, a threshold detector, a maximum aposteriori probability (MAP) detector, a list decoding detector, and a sequential decoding detector.

42. The data detection circuit of Claim 37 wherein said second data detecting means includes:

second finite impulse response (FIR) means for equalizing input data; and

second data detecting means for detecting data in an output of said second FIR means.

43. The data detection circuit of Claim 42 wherein said second data detecting means includes at least one of a Viterbi detector, a decision feedback equalizer (DFE), a peak detector, a threshold detector, a maximum aposteriori probability (MAP) detector, a list decoding detector, and a sequential decoding detector.

44. The data detection circuit of Claim 40 further comprising summing means for receiving an output of said first FIR means, wherein an output of said summing means communicates with said first data detecting means and said baseline correction means, and said baseline correction means outputs said baseline correction signal to said summing means.

45. The data detection circuit of Claim 40 wherein said second data detecting means includes said FIR means and further comprises:

second filter means for filtering using an equalization target with a (1-D) factor and that communicates with an output of said first FIR means; and

second data detecting means for detecting data and that communicates with an output of said second filter means.

46. The data detection circuit of Claim 37 further comprising:

first finite impulse response (FIR) means for equalizing input data;

second filter means for filtering using an equalization target with a (1-D) factor and that communicates with an output of said first FIR means; and

first data detecting means for selecting one of said output of said first FIR means and said output of said second filter means,

wherein said first data detecting means includes said first FIR means and said first data detecting means and wherein said second data detecting means includes said first FIR means, said second filter means and said first data detecting means.

47. The data detection circuit of Claim 46 wherein said first data detecting means includes at least one of a Viterbi detector, a decision feedback equalizer (DFE), a peak detector, a threshold detector, a maximum aposteriori probability (MAP) detector, a list decoding detector, and a sequential decoding detector.

48. A system comprising the data detection circuit of Claim 37 and further comprising:

perpendicular recording means for recording and including read signal preamplifying means for amplifying a read signal;

receiving means for receiving a read signal from said read signal preamplifying means and that communicates with said transient detecting means; and

sampling means for sampling that communicates with said front end.

49. The data detection circuit of Claim 40 wherein said baseline correction means includes:

delay means for delaying and for selectively receiving an output of said first FIR means;

reconstruction filter means for selectively receiving one of said first and second bit streams from said first and second data detecting means, respectively;

summing means for summing and that has a first input that receives an output of said delay means and a second input that receives an output of said reconstruction filter means; and

accumulating means for receiving an output of said first summing means and for generating said baseline correction signal.

50. A system comprising the data detection circuit of Claim 37 and further comprising:

magnetic means for storing data and having sectors, wherein said baseline correction means uses said second bit stream until said sector ends when said transient detecting means senses said transient events during said sector.

51. A data detection circuit, comprising:

thermal asperity detecting means for sensing said thermal asperity events;

data detecting means that communicates with said thermal asperity detecting means for selectively employing a non-DC free equalization target to generate a first bit stream when said thermal asperity events are not sensed and a DC-free equalization target to generate a second bit stream when said thermal asperity events are sensed; and

baseline correction means for generating a baseline correction signal using said first bit stream when said thermal asperity events are not sensed and said second bit stream when said thermal asperity events are sensed.

52. The data detection circuit of Claim 51 wherein said data detecting means comprises first data detecting means for detecting data including:

first finite impulse response (FIR) means for equalizing and that receives input data; and

first data detecting means for receiving an output of said first FIR means.

53. The data detection circuit of Claim 52 wherein said first data detecting means includes at least one of a Viterbi detector, a decision feedback equalizer (DFE), a peak detector, a threshold detector, a maximum aposteriori probability (MAP) detector, a list decoding detector, and a sequential decoding detector.

54. The data detection circuit of Claim 51 wherein said data detecting means comprises second data detecting means for detecting data including:

second finite impulse response (FIR) means for equalizing input data; and

second data detecting means for receiving an output of said second FIR means.

55. The data detection circuit of Claim 54 wherein said second data detecting means includes at least one of a Viterbi detector, a decision feedback equalizer (DFE), a peak detector, a threshold detector, a maximum aposteriori probability (MAP) detector, a list decoding detector, and a sequential decoding detector.

56. The data detection circuit of Claim 52 further comprising summing means for summing and that communicates with an output of said first FIR means, wherein an output of said summing means communicates with said first data detecting means and said baseline correction means, and said baseline correction means outputs said baseline correction signal to said summing means.

57. The data detection circuit of Claim 52 wherein said data detecting means includes second data detecting means for detecting data and including said first FIR means and further comprising:

second filter means for filtering using an equalization target with at least one (1-D) factor and that communicates with an output of said first FIR filter; and

second data detecting means for detecting data that communicates with an output of said second filter means.

58. The data detection circuit of Claim 57 wherein said second data detecting means includes at least one of a Viterbi detector, a decision feedback equalizer (DFE), a peak detector, a threshold detector, a maximum aposteriori probability (MAP) detector, a list decoding detector, and a sequential decoding detector.

59. The data detection circuit of Claim 51 wherein said data detecting means comprises:

first finite impulse response (FIR) means for equalizing input data;

second filter means for filtering using an equalization target with at least one (1-D) factor and that communicates with an output of said first FIR means; and

first data detecting means for selectively communicating with said output of said first FIR means and said output of said second filter means,

wherein when said thermal asperity is not sensed, said data detecting means uses a first data detecting path that includes said first FIR means and said first data detecting means and wherein when said thermal asperity is sensed, said data detecting means uses a second data detecting path that includes said first FIR means, said second filter means and said first data detecting means.

60. The data detection circuit of Claim 59 wherein said first data detecting means includes at least one of a Viterbi detector, a decision feedback equalizer (DFE), a peak detector, a threshold detector, a maximum aposteriori probability (MAP) detector, a list decoding detector, and a sequential decoding detector.

61. A system comprising the data detection circuit of Claim 51 and further comprising:

perpendicular recording means for storing data and that includes read signal preamplifying means for amplifying a read signal;

receiving means for receiving an amplified read signal from said read signal preamplifying means and that communicates with said thermal asperity detecting means; and

sampling means for sampling that communicates with said receiving means.

62. The data detection circuit of Claim 52 wherein said baseline correction means includes:

delay means for selectively receiving an output of said first FIR means;

reconstruction filter means for selectively receiving one of said first and second bit streams from said data detecting means, respectively;

summing means for summing that has a first input that receives an output of said delay element and a second input that receives an output of said reconstruction filter means; and

accumulating means for receiving an output of said first summing means and for generating said baseline correction signal.

63. A system comprising the data detection circuit of Claim 51 and further comprising:

magnetic storing means for storing data and including sectors, wherein said baseline correction means uses said second bit stream until said sector ends when said transient detecting means senses said transient events during said sector.

64. A perpendicular recording system, comprising:

perpendicular recording means for generating a read data signal from sectors of a magnetic storing means for storing data, wherein said read data signal includes at least one of data and transients;

transient detecting means for generating a transient detect signal when said transients are detected in said read data signal; and

detection means for detecting data in said read data signal, for generating a first detected data signal when said transient detect signal is not generated, and for filtering said read data signal and generating a second detected data signal when said transient detect signal is generated,

wherein when transients are detected during a sector, said detecting means continues using said second detected data signal until said sector ends.

65. The perpendicular recording system of Claim 64 wherein said detecting means includes:

a first path including filter means for filtering and first data detecting means for detecting data;

a second path including second data detecting means for detecting data; and

selector means that communicates with said transient detecting means for switching between said first and second paths based on said transient detect signal.

66. The perpendicular recording system of Claim 64 wherein said detecting means includes:

filter means for filtering and including an input and an output;

selector means for bypassing said filter means when said transient detect signal is present;

first detecting means for detecting data and for receiving one of the read data signal from said switch and a filtered read data signal from said filter means.

67. The perpendicular recording system of Claim 65 wherein said first data detecting means includes at least one of a Viterbi detector, a decision feedback equalizer (DFE), a peak detector, a threshold detector, a maximum aposteriori probability (MAP) detector, a list decoding detector, and a sequential decoding detector.

68. The perpendicular recording system of Claim 65 wherein said second data detecting means includes at least one of a Viterbi detector, a decision feedback equalizer (DFE), a peak detector, a threshold detector, a maximum aposteriori probability (MAP) detector, a list decoding detector, and a sequential decoding detector.

69. The perpendicular recording system of Claim 65 wherein said filter means has a high pass filter characteristic.

70. The perpendicular recording system of Claim 64 further comprising discrete channel means for interfacing with said perpendicular recording head and for amplifying said read data signal.

71. The perpendicular recording system of Claim 70 wherein said discrete channel means includes an analog preamplifier, a filter that communicates with said analog preamplifier, and a forward equalizer that communicates with said filter.

72. The perpendicular recording system of Claim 70 wherein said discrete channel means includes:

sampling means for digitizing said read data signal;

FIR filter means for receiving said digitized read data signal from said sampling means, for attenuating out of band noise and for generating an attenuated read data signal; and

equalizing means for receiving said attenuated read data signal and for removing intersymbol interference (ISI) from said attenuated read data signal.

73. A method of operating a data detection circuit, comprising:

sensing transient events in data;

applying a first equalization target to generate a first bit stream from said data;

applying a second equalization target to generate a second bit stream from said data; and

generating a baseline correction signal using said first bit stream when said transient events are not detected and said second bit stream when said transient events are detected.

74. The method of Claim 73 when said transient events are thermal asperity events.

75. The method of Claim 73 wherein said first equalization target is a non-DC free equalization target and said second equalization target is a DC-free equalization target.

76. The method of Claim 74 further comprising detecting data using at least one of a Viterbi detector, a decision feedback equalizer (DFE), a peak detector, a threshold detector, a maximum aposteriori probability (MAP) detector, a list decoding detector, and a sequential decoding detector.

77. The method of Claim 73 further comprising:

reading data from a magnetic medium including sectors; and

using said second bit stream until a sector ends when said transient events are sensed during said sector.

78. A method of operating a data detection circuit, comprising:

sensing said thermal asperity events;

selectively employing a non-DC free equalization target to generate a first bit stream when said thermal asperity events are not sensed and a DC-free equalization target to generate a second bit stream when said thermal asperity events are sensed; and

generating a baseline correction signal using said first bit stream when said thermal asperity events are not sensed and said second bit stream when said thermal asperity events are sensed.

79. The method of Claim 78 further comprising detecting data using at least one of a Viterbi detector, a decision feedback equalizer (DFE), a peak detector, a threshold detector, a maximum aposteriori probability (MAP) detector, a list decoding detector, and a sequential decoding detector to detect data.

80. The method of Claim 78 further comprising:

reading data from a magnetic medium including sectors; and

using said second bit stream until a sector ends when said transient events are sensed during said sector.

81. A method of operating a perpendicular recording system, comprising:

generating a read data signal from sectors of a magnetic storing means for storing data, wherein said read data signal includes at least one of data and transients;

generating a transient detect signal when said transients are detected in said read data signal;

detecting data in said read data signal by at least one of generating a first detected data signal when said transient detect signal is not generated and by filtering said read data signal and generating a second detected data signal when said transient detect signal is generated; and

using said second detected data signal until said sector ends when transients are detected during a sector.

82. The method of Claim 81 wherein said data detecting step uses at least one of a Viterbi detector, a decision feedback equalizer (DFE), a peak detector, a threshold detector, a maximum aposteriori probability (MAP) detector, a list decoding detector, and a sequential decoding detector.